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Linac Upgrade Note **LU-205**

Overview of the Linac Control System

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Attached is Chapter 12 of the Operations Department's "Linac Rookie Book" which covers the Linac Control System as it will be when the 400 MeV Linac Upgrade is completed. This document will be distributed to the Operations Department after the successful completion of the 400 MeV Linac in late CY 1993.

This document provides a detailed and accurate introduction of the Linac Control System. It should be possible to springboard from this document to determine how any of the components of this system work and/or how they can be fixed.

Other documents which describe the system in further detail are listed here.

References

"Upgrading the Fermilab Linac Local Control System," E. McCrory, R. Goodwin and M. Shea, Proceedings of the 1990 Linear Accelerator Conference, Albuquerque, pp474-476.

"Smart Rack Monitor for the Linac Control System", S. Shtirbu, LU-204

"Local Control System Documentation", R. Goodwin, LU-195

"Control System Hardware", M. Shea, LU-206

"Local Applications in the Linac Control System", S. Shtirbu, LU-203

Chapter 12
The Fermilab Linac Control System

Elliott McCrory

The Linac Control System is a modern, modular, synchronous system which provides all access to the hardware in the Fermilab 400 MeV Linac and its associated components. The primary observable function of this control system is to provide the operators with information about the health and well-being of the Linac. This control system is unique primarily because of the unique nature of a linear accelerator: synchronous operation, repeated systems and destructive rf and beam powers. To this end the Linac controls system has the following fundamental features: to inhibit beam before the occurrence of the next pulse of beam if there are any critical devices out of tolerance; to provide accurate, synchronized readings of devices during beam time; to allow the technician working on the equipment to see and modify the local parameters; and to provide modular control for the intrinsically modular Linac systems.

The 400 MeV Linac control system consists of 17 VME crates which control the various subsystems in Linac and which communicate directly with both the Linac Macintosh consoles in the Linac Gallery and with the Vax consoles in the main control room (MCR). The Linac control system speaks with the MCR consoles using the ACNET protocol over token ring. Each VME local control station (LCS) is a front end; one LCS acts as a data server between the information in the various Linac sub-systems and the consoles in the MCR. Data are obtained for an LCS from the Linac sub-systems through Smart Rack Monitors (SRMs) which are connected to an LCS by the Arcnet local area network.

The controls software in both the LCS and the SRM runs from information specific to that module obtained from tables in non-volatile random-access memory (NVRAM) at that module. The multi-tasking pSOS operating system directs a small number of tasks to perform the controls operations so that all activity is completed between linac beam pulses, at15 Hz (66.7 ms. apart).

12.1 Layout of the control system.

Figure 12.1 shows the topology of the Linac Control System. The LCSs are distributed as follows: One for the pre-accs and the 750 keV lines, two for the 201 MHz on-line systems, one for NTF, one for the MCR "Linac Alarms Screen," one for the linac data server (a.k.a., the linac front end), nine for the 805 MHz rf systems, one for the upgraded-linac diagnostics and one for the upgraded-linac trim and quad magnets.

These LCSs communicate with each other, with the Linac Macintosh consoles and with the MCR Vaxen via IEEE 802.5 Token Ring. Each LCS is an equal partner on the network, able to obtain

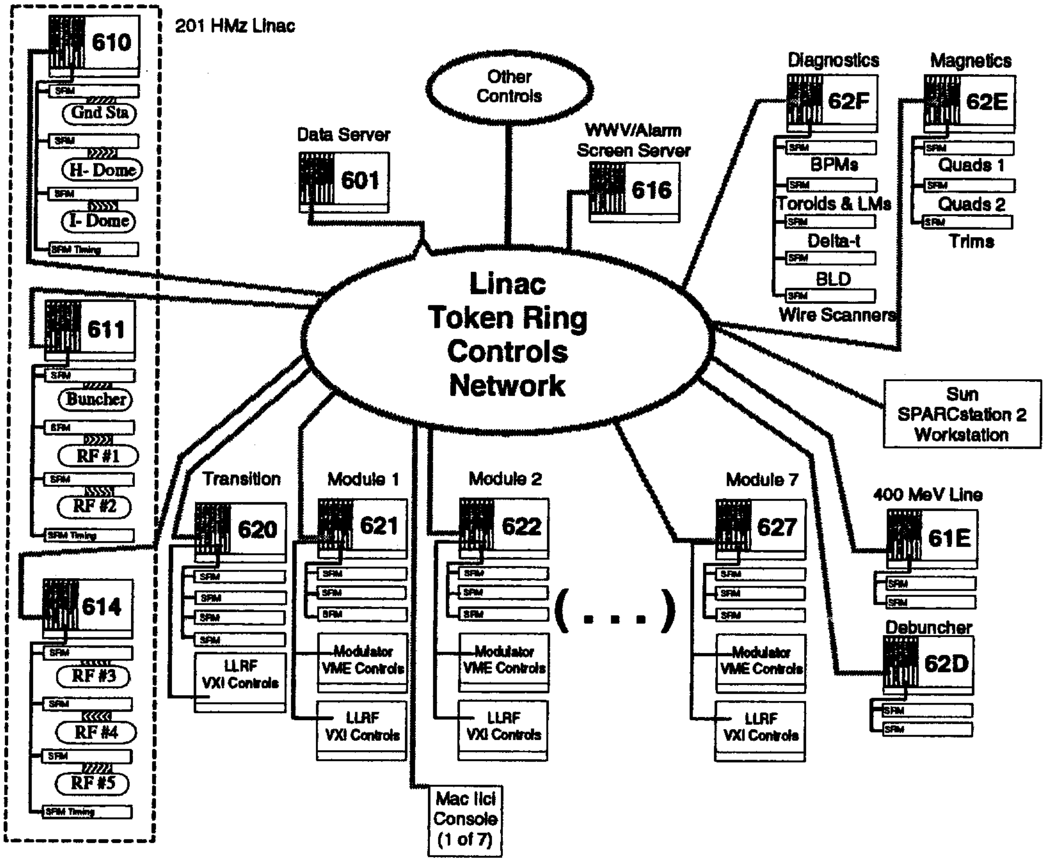


Figure 12.1, Layout of the Fermilab Linac Control System.

data from and to reply to any other node on the network. All hardware from the LCSs is entirely interchangeable. The controls software is the same in each LCS.

The various Linac sub-systems are referred to in the following manner:

Name	**Node**	**Description**
H	610	H- Ion source ("H- dome" or "H- Haefley")
I	610	I- Ion source ("I- dome" or "I- Haefley")
G	610	Ground Station/750 KeV Line
B	611	RF System for the Buncher and the emittance probes
1, 2	611	RF System for Tank 1, 2
3, 4, 5	614	RF System for Tank 3, 4 and 5
K0	620	RF System for Transition Section 0
KV	620	RF System for Transition Section Vernier
K1-K7	621-627	RF System for Klystron #1 through Klystron #7
KD	62D	RF System for the Debuncher
Mags	62E	Quads and Trim Magnets
Diags	62F	Upgraded-linac Diagnostics
E	61E	200 MeV line devices
C	61C	NTF
A	61A	RF System for the 201 MHz test station

The node number is the last 2 bytes of the token ring address of the LCS which controls that sub-system. This number is expressed in base 16 (hexadecimal).

The VME stations and their little consoles are located as follows:

Node	Location (Little Console Location)
601	At RF Station 1 (no little console)
610	At the Haefley Controls, ground station (G)
611	At RF Station 1, above node 601 (RF1)
614	At RF Station 4 (RF4)
616	At RF Station 6 (RF6 & MCR)
620-62F	At Klystron RF Stations 0 through 7 (At 0, 2, 4, 6, and 7)
62D	Booster Lab 7 Debuncher (Lab 7)
62E	Just South of Linac Diags Room (no little console)
62F	Linac Diagnostics Room (in Diags Room)
61E	In the racks just beyond the linac gallery, 200 MeV line (E)
61A	At the 201 MHz Test Station (A)
61C	In the Linac basement at NTF, south side (C, basement)

The token ring network is logically divided into four lobes. They are (1) the global ring, (2) the DZero ring, (3) the local ring and (4) the linac ring. (3) is where all the Controls Vaxen, and front ends sit.

12.2. A VME Local Control Station

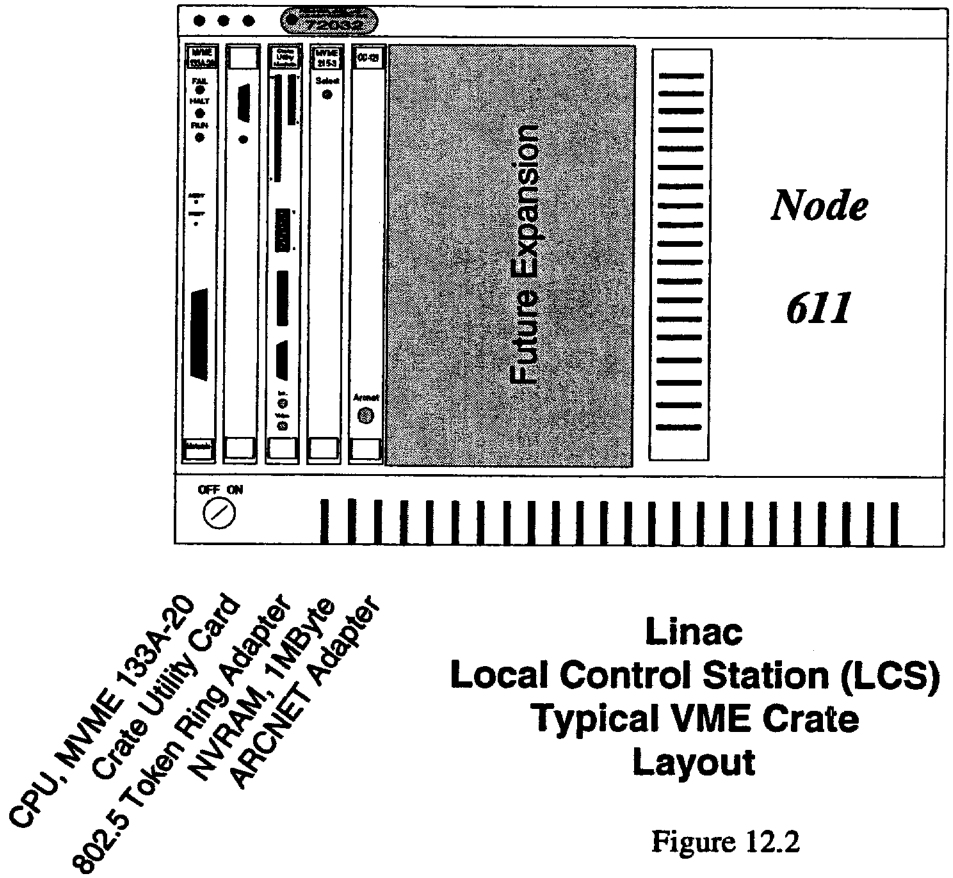
The VME local control stations, as listed above, each function as a full-fledged control system. Each LCS consists of a CPU, two network adapters, non-volatile memory, and a catch-all utility card in a 12-slot VME crate. See Figure 12.2. All cards except the utility card are commercially available.

In the left-most slot of the VME crate is the MVME 133A-20 cpu card which contains the MC68020 cpu, some volatile memory, a serial (RS232) port, and other functions. The other cards in the VME crate are (generally left-to-right in the crate): the token ring adapter made by Proteon, a locally-made Crate Utility Card, a 1MB non-volatile (battery-backed) RAM card, an Arcnet adapter and possibly other cards, like a 4-channel quick (2 MHz) digitizer. The interface to the Linac hardware is via the Arcnet network to SRMs, see below.

There are three local copies of the code which the local computer uses for the system: the one it is running from volatile memory, a copy in NVRAM which it reads when the cpu is reset, and a copy in PROM which it will use if the NVRAM copy is faulty. If the system gets an unrecoverable error or if a watchdog timer (on the Crate Utility Card) expires, the system will try to reset itself. If the problem still exists when the system returns, then after 15 tries, the system will try no more. An expert would need to be called in this case.

12.2.1 15Hz Activity

The MC68020 computer is responsible for the following list of activities, which it performs within the 66.7 milliseconds between Linac beam pulses:



Linac
Local Control Station (LCS)
Typical VME Crate
Layout

Figure 12.2

0. Receive an external interrupt saying that the 15Hz clock has just ticked;
1. Execute the *Update Task*
2. Scan analog devices and binary status for alarms;
3. Service the PA running on the little console;
4. Execute the *Server Task* (at 40 ms).

12.2.2. The Update Task

The Update Task is very important. It is not necessary to understand all of the details of its operation to understand its function, but some details are pertinent. Information in the LCS is stored in NVRAM in the form of various tables. One table, the RDATA table contains the list of operations to be performed by the Update Task each cycle. The order of execution corresponds to the order of information in the table. In the Update task, it takes between 11 and 20 ms to process the RDATA list. Typical RDATA table entries in a Linac LCS do the following:

1. Tell the SRMs, by issuing an Arcnet broadcast, that their data are needed;
2. Recover the data from the SRMs and perform the next two steps with these data;
3. Update readings for all analog devices;
4. Update readings for all binary I/O data;
5. Update the other, more obscure sorts of data kept by the system (e.g., datastreams);

6. Perform zero-data, linearization, derived channels, etc. as appropriate;

7. Let all the Local Applications (LAs, see below) run.

After RDATA processing in the Update Task, all currently active non-server data requests due this cycle are fulfilled for network requestors. In other words, if a console somewhere is expecting data from an LCS, then that information is sent over the network at this time.

A network requestors can cause the system to reply, asynchronously, at any time, although it will not reply right away if it is busy. An LCS should always respond within 40 ms, even in a worst case, but it can be as short as 5 ms. The systems generally have at least 45 msec of idle time per cycle.

12.2.3 Local Data Base

Each LCS has a local data base which describes the attributes of each analog device and of each bit of binary I/O. (This information is located in the ADESC and the BDESC tables, respectively.) This database exists in parallel to the centralized ACNET database. It is possible for the technician in the field to modify the local database to suit his or her immediate needs (*e.g.*, s/he discovers that the conversion constants are not correct for the device; ususally done on "Page A" or EDAD, see below.). Therefore it is important to know that if changes are made locally, the *Linac Controls Liaison* needs to be notified to upload the Linac database into the central database. This operation is simple and quick. There is not, at this time, a procedure for downloading the central database to the LCSs.

All of the information described here is stored in NVRAM on the separate 1 MByte NVRAM VME card in the LCS. This information should survive a power failure. The Linac Controls experts have copies of the local database in a safe place where it can be restored in a catastrophy. This information is what makes the systems behave differently from one another. A complete list of the types of tables in a LCS is given in Table 12.1.

12.3. The Linac Data Server and the Interface to the MCR Consoles.

One of the VME LCSs, node 601, is responsible for consolidating the data flow between the Linac LCSs and the MCR consoles. This LCS sometimes is called the Linac Front End and sometimes is called the Linac Data Server (LDS). It is needed because it has been observed that several remote systems trying to report data back to a console at 15 Hz will cause the console to fail. The LDS has no trouble performing this task for the consoles. (Since front ends have been typically thought of as a protocol-translating network computer *e.g.*, ACNET-to-Camac or ACNET-to-SDLC, then the LDS is really not a front end.) The LDS gets a message directly from a MCR console and distributes the message, essentially unchanged, to the proper LCS(s).

Special code has been added to each LCS to service the multi-purpose parameter page in the MCR. Each LCS averages 15 readings, paying attention to the presence or absence of beam, and reports a 1 Hz average back to the parameter page. The LDS passes this information unmodified.

All Linac LCSs understand the ACNET protocol, for example SETDAT, RETDAT and

Table 12.1, Linac Controls LCS System Tables

Table #	Name	Description	Size
0	ADATA	Analog Channel Dynamic Values	16
1	ADESC	Analog Descriptor	64
2	BALRM	Binary Alarm Flags	4
3	BDESC	Binary Descriptor	16
4	RDATA	Read Data Access Table	16
5	BBYTE	Binary Status Bytes (Binary Data)	1
6	PAGEP	Page Pointer (Local software)	20
7	PAGEM	Page Memory (Private memory)	128
8	LISTP	Active Data Request Ptr	8
9	CODES	For downloading software	32
10	CDATA	Comment Alarm Data (Sys Reset)	32
11	BADDR	Binary Byte Address	4
12	OUTPQ	Output Pointer Queue (Network)	8
13	PRNTQ	Serial Output Queue	4
14	LATBL	Local Applications	32
15	CPROQ	Co-processor Queue Pointers	16
16	MMAPS	Memory-mapped template (D0)	8
17	Q1553	1553 Controller Queue Pointers	4
18	DSTRM	Data Streams	32
19	SERIQ	Serial Input Queue	1K
21	AADIB	Analog Alarm Device Info Block (D0)	32
22	BADIB	Binary Alarm Device Info Blocks (D0)	32
23	CADIB	Comment Alarm DIB (D0)	32
24	CSTAT	Combined Binary Status	32
28	IPARP	Internet Security	16
29	DIAGQ	Alloc, Liber Diagnostics	16
30	TRING	Token Ring Network	8K

FTPMAN. One could modify the ACNET database entries for the Linac devices to entirely bypass the LDS, if one were interested in the absolute fastest turn-around between the Linac and the operator in the MCR.

Node 616 is a special node. It does no data acquisition. It performs two functions: (1) to watch the network for prompt Linac-type alarms and place them on the monochrome Linac alarms screen in the MCR, and (2) run the little console in the MCR.

Node 610 listens to the short-wave radio station WWV and provides highly accurate time-of-day information to anyone on the network who cares to listen. All LCSs listen for this information and synchronize their internal clocks to it. The time field on the monochrome Linac alarms screen and in the upper-right-hand corner of the screen on the little console reflects this accurate, synchronized time.

Fermilab Linac Control System Smart Rack Monitor (SRM)

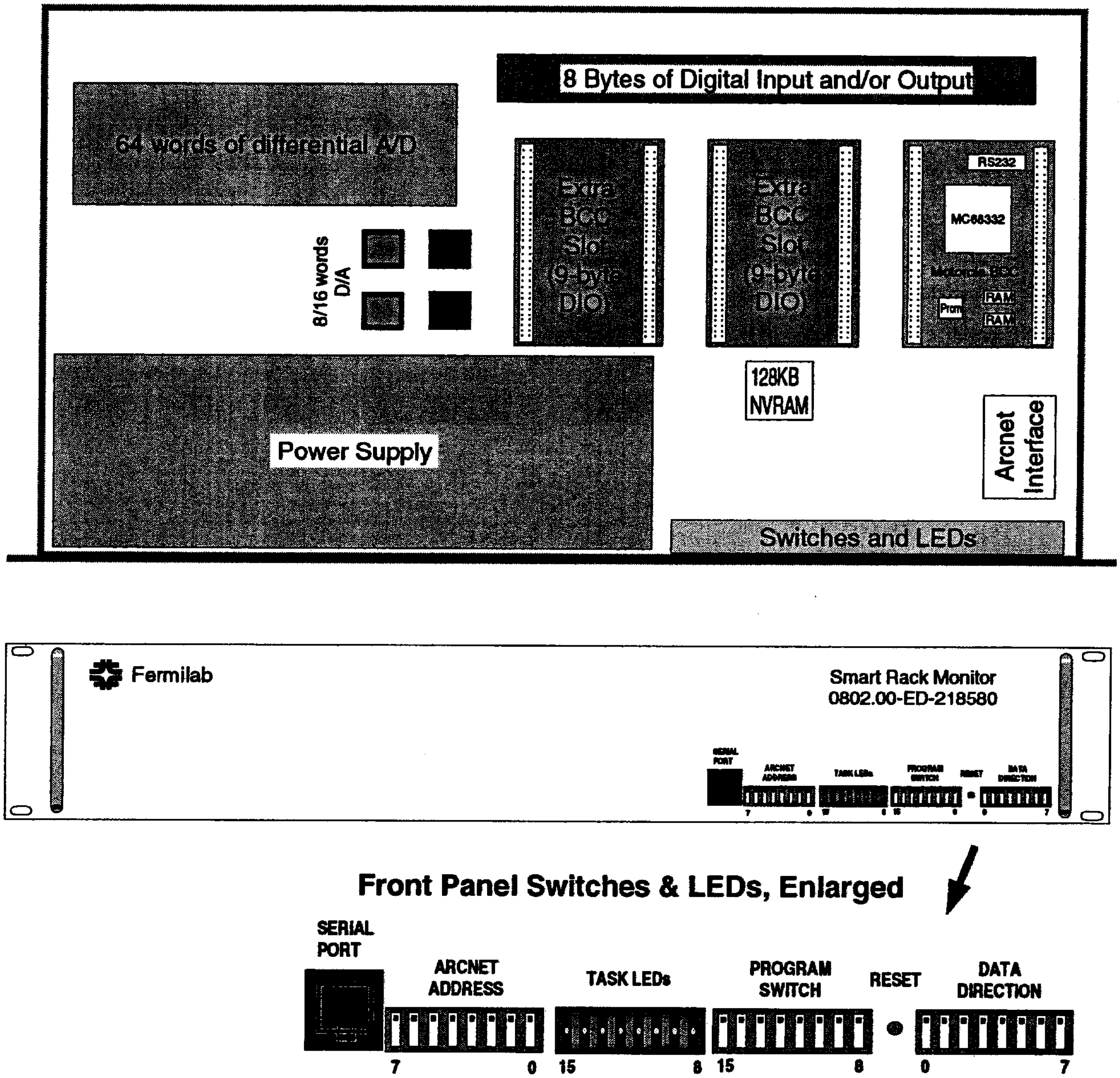


Figure 12.3, SRM Block diagram

12.4. The Smart Rack Monitor

All of the routine, low-level data gathering is done by Smart Rack Monitors (SRMs). A block-diagram for this device is shown in Figure 12.3. An SRM is a 2U (3.5") 19"-wide chassis that contains 64 16-bit differential A-D channels, 8 or 16 12-bit D-A channels, 8 bytes of digital I/O, 256k bytes of nonvolatile RAM, an Arcnet adapter and a processor. The processor is on a Motorola Business Card Computer (BCC) that includes an MC68332 processor, 64k bytes of RAM, 128k bytes of

PROM and a serial port. There are three sockets on the SRM motherboard into which the BCC can be installed.

Several other boards have been designed and built at Fermilab to fit into the other BCC sockets. A card which contains exactly the same functionality of the (retired) Multibus-I 9-byte digital I/O cards used in the old Linac Control System has been built. One of these cards in an SRM allows the SRM to access the 16-channel A-D chassis, the 16-channel D-A chassis and the Modulator Diagnostics at a Linac sub-system. This is the "red dot" board. The other 9-byte DIO card, the "blue dot" board, is used to perform normal binary I/O. There is also a BCC-size Tevatron clock decoder in some SRMs which allows an LCS to be synchronized with the rest of the Linac.

12.4.1 Types of SRMs

According to the type of hardware and data tables loaded into the SRM, we have 4 types of SRM in the Linac (the software is the same in each). These SRMs are distributed as follows in the Linac (the Arcnet column is the Arcnet address of the SRM, in Hex):

Linac Controls SRM Details

Node	Location	Arcnet	Type of SRM
610	G, Ground Sta.	A1	A/D, D/A & Binary
610	G, Ground Sta.	A5	LCLK generator
610	G, Ground Sta.	A4	Timers, on-board D/As
610	I- Dome	A3	Fiber optic Arcnet; Timers, A/D, D/A, Binary, Old DIO
610	H- Dome	A2	Fiber optic Arcnet; Timers, A/D, D/A, Binary, Old DIO
611	RF for Buncher	A1	A/D, D/A, Binary, Old DIO
611	RF for Buncher	A4	Timers, A/D, D/A, Old DIO
611	RF Sta #1	A2	A/D, D/A & Old DIO
611	RF Sta #2	A3	A/D, D/A & Old DIO
614	RF Sta #3	A1	A/D, D/A & Old DIO
614	RF Sta #4	A2	A/D, D/A & Old DIO
614	RF Sta #4	A4	Timers
614	RF Sta #5	A3	A/D, D/A & Old DIO
620	Transition Sect'n	A1..A6	A/D, D/A, Binary, Timer
62n	Klystron 1-7	A1, A2	A/D, D/A, Binary, Timer
62n	Linac Basement	A3	Water Skid: A/D, D/a, Binary
624	Comm Rack	A4	LCLK Generator
627	Klystron 7	A5	Ion Pump Interface
627	Klystron 7	A4	Valve Control Interface
62E	Througout Gall'y	A1..A4	A/D, D/A, Binary, Timing
62F	Diags Room	A1..A4	A/D, D/A, Binary, Timing
62D	Debuncher		Same as Transition Sect'n
61E	200 MeV line	A2	A/D, D/A & Old DIO
61E	200 MeV Line	A4	Timers, on-board D/As
61E	RF for Debun.	A3	A/D, D/A & Binary interface

12.4.2 15Hz Activity in an SRM

The control program in the SRM has a list of tasks to perform, modeled after the system software in the LCS. The information is stored in tables, including the information on what to do during the SRM's Update Task. A typical list of tasks performed by an SRM is as follows:

1. Wait for the parent LCS to ask for data;
2. Direct the on-board digitizers to do their thing;
3. Read the on-board digitizers;
4. Direct the old A/D hardware to digitize;
5. Read these data;
6. Read the binary information (on-board and through 9-byte DIO card);
7. Place the data into the appropriate places in local memory;
8. Reply to the parent LCS with the answers;
9. Be prepared to reply to asynchronous settings messages.

The SRM has been measured to perform this set of tasks in about 10 ms.

The SRM also has three copies of its code, and tries to recover from unexpected problems by copying a backup copy of the code and resetting. After four tries, the SRM tries to execute the code from the PROM. If this fails, the SRM gives up and waits for help. Pressing the reset button on the front panel of the SRM causes it to retry one more time, but if the cause of the problem was not fixed, the SRM will give up again.

12.5 External Hardware

The external 16-channel, 12-bit, sample-and-hold A/D converters are used to digitize analog signals in the old Linac sub-system (G, H, I, 1, 2, 3, 4, 5 and A). Each sub-system has one to six of these A/D converters. Usually, all the sample-and-holds in the Linac are triggered simultaneously by the `L:TDATA` timing pulse, which is generated at sub-system B. The analog range of these A/Ds is generally -10 to 10 volts. The sub-systems which control rf stations (B, 1-9, and D) also have one A/D chassis with an input range of -2.5 to 2.5 volts for 4x increased resolution of rf signals. The Linac beam position monitors, located at 2-9 and E, also are also digitized by 2.5 volt A/Ds.

All the old sub-systems also have external 16-channel, 10-bit D/A converters of 0-10 volt outputs. These are used to control linac quadrupoles and 750 KeV line devices.

The upgraded-linac stations use the A/D's and D/A's on board the SRMs.

The dipole trim magnets and stepping motors are driven by the SRM on-board D/As and DIO. Trim magnets are located at G, 3, E and Mags. There are two types of trim magnet power supplies. 8-output power supplies are at 3 and at Mags and are identified by two rows of BNC connectors on the front and a column of red LEDs on the right hand side of the chassis. These have a limit of +6 to -6 amps. The trim magnets controlled by this type of ps are called `L:xTyzzz` where `x` is `H` or `V`, `y` is a digit 2 through 5 and `zzz` is `IN` or `OUT`. For example, `L:HT4IN` is the horizontal trim at the input to Tank 4. The other type of power supply has a range of +10 to -10 amps. This PS is a 19" supply which controls a single trim magnet. These are located at G (`L:TRIM90`) and at E (`L:HT2001` through `L:VT2002`).

12.6 Interface to the Upgrade Modulator and LLRF Systems

The modulator and low-level rf systems in the Upgraded Linac are controlled by, respectively, local VME and local VXI systems. Communications with these systesm is accomplished over a Vertical Interconnect (VI). This locally-made VME device maps 24 MBytes of VME backplane memory from the slave VME/VXI crate to the master LCS in an essentially transparent manner. The system code in each sub-system is organized in such a way that all the analog and digital readings and settings are within that 24 MByte window in a way that is well known to the LCS experts.

Each sub-system is responsible for incrementing a local counter which the LCS system software inspects at 15 Hz to be sure that counter is incrementing. If this counter is not incrementing, it is a reasonable guess that the low-level processor is not behaving properly. In this cane, the device `L:MnHB` or `L:LnHB` (for Modulator or LLRF, respectively) will alarm. (`HB` stands for Heart Beat.)

Further description of these systems can be found elsewhere.

12.7 Linac Timing

Linac uses the Tevatron clock, TCLK, to generate timing pulses for the linac. Two special SRMs exists to handle this function: one at the Ground Station and one at the Comm Rack near the modulator for klystron #4. These SRMs contain a BCC with an ACTEL 1020 gate array configured to generate a TCLK-like signal and to back it up, using a local 10 MHz oscillator, on those rare occasions when TCLK is down. Thus, NTF can continue to run if TCLK is off. On the back of this SRM are lemo spigots which allow PREDET-type signals to be connected to generate clock events on the local clock. This local clock is referred to as LCLK. The events presently used are:

Event	**Description**
`$AF`	Booster Reset (regular 15 Hz)
`$AE`	Pulse Shifter (15 Hz for the ion sources)
`$A7`	Klystron 15Hz, Charge
`$A6`	Klystron 15Hz, Fire
`$A5`	Klystron Reduced-rate, Charge
`$A4`	Klystron Reduced-rate, Fire
`$A3`	Upgrade Quad Sample Time
`$A1`	Low-Level RF Trigger

One of the SRMs at each LCS is dedicated to receiving LCLK. This SRM is loaded with a BCC similar to the one at the Ground Station. It also contains an ACTEL 1020 gate array, but this one is configured to accept LCLK (or TCLK) and to output properly timed pulses. Up to four delayed outputs, i.e., μP start, can be triggered from one event. Four clock events can be selected as outputs (determined by PALs). The timing SRM also serves as a clock (TCLK or LCLK) repeater, providing two copies of the clock.

The analog devices which describe these events are located in the LCS database beginning at channel number `0x080`. The devices are named as follows:

Name	**Title**	**Description**
`L:RF`*n*`T0`*m*	`RF`*n* `TIMER` *m*	Delay for this pulse
`L:RF`*n*`EV`*m*	`RF`*n* `EVENT` *m*	Event on LCLK which triggers this pulse
`L:KnT0m`	`Kn TIMER m`	(Upgrade) Delay for this pulse
`L:KnEVm`	`Kn EVENT m`	(Upgrade) Event on LCLK which triggers this pulse
`L:KnCNm`	`Kn CONTROL m`	(Upgrade) Control word

The device `L:TDATA` would be, logically, `L:RF1T00`, but the old name has been retained.

12.8 ACNET Interface to Binary Status Information

The Linac sub-systems each contain several dozen bits of digital status. These bits are read in groups in a manner similar to the way bits are read in other parts of the complex. These combined binary devices can be read on page S53 just like other binary information.

These devices can be set to alarm and to inhibit beam, as can the analog devices in the Linac control system. They are reported on the Linac alarms screen in the normal manner, and they appear on the AEOLUS alarms screen as digital alarms. These alarms should *not* be ignored. An operator should ***not*** nominalize these devices . At this time, none of these combined binary devices is set to inhibit beam.

The nominal value for these devices is only pertinent when viewed as a raw hexadecimal value. This is the expected bit pattern for the bits in this device. The tolerance value, again viewed as a hexadecimal number, is considered to be a mask; the bits that are 1's are the bits which are observed in the alarm scan.

Note that this is the only way in which binary information produces an AEOLUS alarm in the Linac control system. This is different from the recent past; the change was made at the same time as the Linac controls upgrade at the request of the Operations Department. Many of these bits are very important, so it is critical that all operators learn how to understand the alarm messages produced by these bits.

The combined-binary devices in the 201 MHz RF sub-systems at this time are: RnMISC, RFnVAC, RFnPA and RFnDRV. The combined binary devices in the 805 MHz RF sub-systems are: BnLCS, BnILK1, BnILK2, BnDIS1, BnDIS2, BnSOL, BnCOIL, BnLLRF, BnWATR, BnMODR and BnMOIL.

12.9 Local Applications

Each LCS has the ability to run customized closed-loop applications at the end of the Update Task. These application, called Local Applications or LAs, are independant programs, written in Pascal or C, which can control anything at the LCS. The LAs currently in use are:

Name	Description
GRAD	Regulates gradient in the 201 MHz tanks
PHAS	Regulates inter-tank phase in the 201 MHz tanks
CROB	Recovery from PA crowbar
DRIV	Recovery from driver trips
PINH	Reduction of gradient after trip without recovery
QUAD	Recovery of DTL quad PS trip
PRES	Regulate ion source pressure
NETM	Lost network recovery
AERS	AEOLUS shepherding
FTPM	FTPMAN support
AAUX	ACNET AUX support
GATE	ACNET-header gateway support to SRM
TEMP	Regulate water temperture in side-coupled cavities (SCC) modules
FREQ	Controls VCO to keep SCC resonant
EMIT	Emittance probe and wire scanner control

All routine failures of the hardware in the Linac sub-systems are handled by these programs. For example, the LA NETM watches the token ring network activity at the LCS and tries to bring it back online if the network or the LCS should fail.

12.10 Alarms and Beam Inhibit

Each LCS can inhibit beam by pulling down on a line which runs throughout the Linac. This is capable of happening during any 15 Hz cycle, but it should only happen when a device is out of tolerance or when a station dies. This common line is wired into the backplane of the VME crate.

Prompt Linac-type alarm messages, which appear on the monochrome screen above Console 1 in the MCR, and slow AEOLUS alarms are issued by each of the LCSs. In the MCR, sub-page J of page L22 allows the operator to reset the alarms from each LCS individually. This is in addition to the normal "blue button" interrupt on the alarms screen console application.

12.11 Other Features

There are several, more obscure features of the Linac control system, which will be listed here. Each device can be made to wait for up to 15 consecutive bad readings before reporting an alarm.

Many devices, most notably the BPMs, are read out through a 1 to 5 MHz Quick Digitizer. It is desired to eventually allow these channels to be read out through the Snapshot mechanism.

Each LCS contains a binary datum, usually at bit number 0x0A7, which controls whether or not that station is to report alarms on the network. *This bit should always be tunred on!* There is a special case in the alarms reporting algorithm which will report an alarm if this bit is turned off.

The beam enable line is split at Tank 4 into upstream and downstream halves. The downstream half is held high by a power supply at the ground station; at the upstream end, it is held high at the location of the old debucher racks. Any LCS can pull it low to inhibit beam.

12.12 Checklist

There is an independant checklist program, running on the Linac Department Sun computer okra, which checks several aspects of the control system which whould never break, but would provide a logical loophole for catastrophy if they were to break. These items are (at this time):

Are the expected stations answering to simple network requests?
Would the local control stations report that 'alarms reporting' is turned off?
Is the system code in each station reasonably up-to-date?
Are there any binary data which could inhibit beam silently?

This checklist program runs every day at 16:00 and the output is sent to a Linac Staff member. Other item are added and removed routinely.

12.13 Trouble Shooting

Every LCS and every SRM has diagnostic LEDs on its front panel. The most interesting LEDs on the VME are on the crate utility card. These LEDs should be flashing at 15Hz. If there are no 15 Hz interrupts to the system, then they will flash at 12.5 Hz. If you are standing in the Linac gallery, then you can hear 15 Hz--it is easy to notice if the computer is not synchronous to this sound.

A complete set of ACNET error codes, facility code 36, can be obtained from the *Linac Controls Liason.*

The SRM LEDs should also be flashing at 15 Hz. If an SRM is disconnected from its LCS or if its LCS is not getting 15 Hz interrupts, the SRM LEDs will flash at 12.5 Hz.

In general, it is not appropriate for a non-expert to change an SRM because the software in the SRM will need to be changed, too. The module itself can be switched with one of the same type (# on a sticky label on the front panel of the SRM). Before connecting the replacement to the network, the SRM dip-switches on the front panel should be changed to match the configuration of the removed SRM. If, after turning on the SRM, the LEDs flash at 15 Hz, then the SRM is okay, but it may still require some changes in its local tables. This is what requires an expert.

The Linac timing system runs off of TCLK. If there is a glitch in TCLK, then we may miss a 15Hz clock tick. The LCSs will not wait forever for the tick, so after 80 milliseconds the software will generate an artificial tick. Since this tick is asynchronous, many devices (e.g., the quads) will be out of tolerance at that particular time. Look for a devices called `L:nS15HZ` for the 201 MHz linac and `L:ZnHZ15` for the 805 MHz Linac. This device measures the length of the cycle; if it is not 66 or 67 milliseconds, then it will alarm.

A particularly obnoxious mode which seems to be a failure is when, for whatever reason, the LCS sees a very large number of alarms over a short period of time. (We have observed many thousand alarms in about a minute.) AEOLUS is not designed for this volume of error messages, so it may take a long time for all of these alarms to clear out of the system. The monochrome linac alarms screen may not even be able to keep up. The key to identifying this type of situation is when the monochrome linac alarms screen is continuously scrolling and the date stamp on the alarms messages is not synchronous to the WWV time as seen in the MCR. The only real solution is to verify that the initial problem is fixed (whatever that may be!) and wait. The two situations in which this has been observed are: (1) TCLK interruptions and (2) power glitches.

12.14 Linac Macintosh Consoles

Several Macintosh computers, model IIci, have been purchased to replace some of the little consoles. Extensive controls software has been written for this platform. The applications currently available which can access linac data are:

1. Parameter page (note that "`L:`" is not part of the device name)
2. Time plot, knob plot and VME memory plot package
3. VME memory dump page
4. VME screen image ("Page G")
5. LabView

These programs adhere scrupulously to the Macintosh "look-and-feel" and are quite easy to use. A detailed tutorial is available elsewhere.

In order to make settings from one of these applications, one must enter the proper password. This is the "Enable Settings" option in the "Options" pull-down menu.

Item #4, "Page G," is what will make the little consoles obsolete. Since all of the functionality of the little console can be obtained through VME memory, and since VME memory is easily accessible to the Mac, an application can be written to exercise this memory in such a way as to put the image and the functionality of the little console on the Mac. One can accurately think of this as analogous to the X-Windows client/server model, where the client is the virtual little console at the VME system and the server is the Mac screen. You must "Enable Settings" to do anything except look at the existing screen image. This program can be run even if the little console does not actually exist at the LCS.

12.15 The Little Consoles

The device which is referred to here as "the little console" is the small 19"-rack-mounted crt/keyboard which the technician can use to look at and modify parameters while working on the various Linac sub-systems in the field. All of the old linac sub-systems (G, 1, 2, 3, 4, 5 and E), klystrons number 0, 2, 4, 6, 7 and D, the Diagnostics Room and the MCR each have a little console. There are also several others scattered around the Accelerator Division. These consoles useful locally, as mentioned above, and crucial for when the LCS drops off of the token ring network, when a new LCS is being set up or when major changes are being made to an existing LCS. It should not be necessary for operators to ever use these consoles.

The most used application on the little console is the parameter page. The first line of the display contains a title, the date and the time. The rest of the lines, excluding the last line, are available for parameter viewing. Enter the 6-character name of the device (without the `L:`), or the channel:node number. For example, `GR1MID` or `611:302`. Use the red key labeled "INTR" on the face of the little console, or use the "ESC" key or any other key marked with "INTR" to perform the operation. The RETURN key does a carriage return, not an interrupt. To change the setting of a device requires that the key be inserted and turned so that the red LED is on. A device setting can be changed in one of three ways: entering a new value and hitting "INTR;" pressing the green up/down keys on the face of the little console;

LCS Primary Applications

Name	Page	Description
PARM	various	Local parameter Page
EDAD	A	Analog descriptors, change local analog database
EDBD	B	Binary descriptors, change local binary database
LAPP	E	See parameters associated with the local applications
FRAM	F	See network frames (Does not appear on index page)
CRTI	G	Little Console image across the network ("Page G")
SRMC	H	Copy memory to and from an SRM
MBLK	K	See pSOS-allocate VME memory
ACRQ	L	ACNET protocol data request test
MDMP	M, N	VME memory dump
SURV	Q	Roll-call on network of LCSs
TRNG	T	Token Ring initialization page

or by using the knob. Other details of the operation of this program can be found elsewhere.

Some of the avaliable applications are listed here (although they are not necessarily all loaded on each LCS).

(Note: If you need to use these programs, please consult an expert for a tutorial first. These applications interface with the Linac control system in a way which is subtly different from the applications on an MCR console. Be especially careful with EDAD, EDBD and MDMP.)

All of the application on the little console can be run from a Macintosh when the LCS is on the network. This is accomplished via the "VME Screen Image" application on the Mac.

This document is judged to be an accurate and complete description of the Linac Control System as of today, April 21, 1993.

Signed ____ Date ______________

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